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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,934	03/06/2002	Amir Alon	IL920020007US1	7058
7590 06/03/2005			EXAMINER	
IBM CORPORATION INTELLECTUAL PROPERTY LAW DEPT. P.O. BOX 218 YORKTOWN HEIGHTS, NY 10598			LEVIN, NAUM B	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No. 10/091,934	Applicant(s) ALON ET AL.	
	Examiner Naum B. Levin	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-9, 11-18 and 30-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-9, 11-18 and 30-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/091,934 and Amendment filed on 03/03/2005. Claims 2-9, 11-18, 30-35 and 36-41 remain pending in the application. Claims 30-32, 34 and 35 have been amended by including additional limitation.

Based on the remarks and Amendment Examiner has performed additional search, and found new references.

Claim Objections

2. Claim 30 is objected to:
the recitation of "said chip architecture" is not clear to what applicants intend to mean.

3. Claim 32 is objected to:
"circuits (IC)" should be replaced with – circuit (ICs).

4. Claims 34-35 are objected to:
Applicants must clarify what is "parameterized cells".

5. Claim 36 is objected to:
Applicants must clarify what is "parameterized design topologies".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2- 9, 11-18, 36-37 and 38-35 are rejected under 35 U.S.C. 102(e) as being unpatentable by Saito (Pub. No.: US 2002/0095648).

As to claims 2, 6, 15, 17, 30, 31, 32, 34 and 35 Saito discloses Layout method of analog/digital mixed semiconductor integrated circuit including:

(2) An integrated circuit design kit/system comprising:

means (tools/simulators/synthesizers) for generating one or more circuit component topologies (layout) ([0032]-[0033]); and

means (tools/simulators/synthesizers) for designing one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout), for analog and mixed signal (AMS) circuit (digital and analog subsystems in one circuit) design ([0037]);

(6) A design topology (layout) of AMS transmission lines (interconnects/wires/critical signal nets/critical paths) ([0037]);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines ([0032]-[0033]; [0037]);

(17) A computer software circuit design product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy

said circuit design product, said circuit design product comprising means for designing topology of transmission lines ([0032]-[0033]; [0037]);

(30) A method for designing integrated circuits wherein defining a chip architecture and a floor plan comprises defining critical interconnect wires ([0032]-[0034]; [0037]);

(31) a system for integrated circuit design comprising:
means (tools/simulators/synthesizers) for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks (macros) and their locations are defined, and further including one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout) ([0032]-[0034]; [0037]);

means (tools/simulators/synthesizers) for designing a schematic design at least including one or more circuit components and one or more transmission lines models ([0032]-[0034]; [0037]); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more transmission line topologies ([0032]-[0034]; [0037]);

(32) A method for designing integrated circuits (IC), said method comprising steps of:

- a) defining a chip architecture and floor plan ([0032]-[0034]; [0037]);
- b) identifying one or more critical interconnect lines/wire and defining one or

more transmission line topologies for said critical interconnect lines ([0032]-[0034]; [0037]);

c) determining a schematic design (logic gate level circuit description) of said IC from said chip architecture, floor plan and said transmission line topologies ([0032]-[0034]; [0037]); and

d) defining a physical layout of said IC at least from said chip architecture, floor plan and said line topologies ([0032]-[0034]; [0037]);

(34) A system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more transmission lines models, wherein said one or more transmission lines are models parameterized cells of one or more transmission lines topologies ([0032]-[0034]; [0037]; [0041]- [0042]);

(35) A method for designing integrated circuits (IC), said method comprising:

means (tools/simulators/synthesizers) for designing a schematic design ([0032]-[0034]; [0037]); and

means (tools/simulators/synthesizers) for designing a physical layout including at least one or more circuit components and one or more transmission line topologies, wherein said one or more transmission line topologies are parameterized cells of transmission lines ([0032]-[0034]; [0037]).

As to claims 3-5, 7-9, 11-14, 16, 18, 36, 37, 38-41 and 33 Saito recites:

- (3), (7) The kit wherein said transmission line topologies are predefined ([0036]);
- (4) The kit of claim 2 further comprising one or more circuit component models ([0036]);
- (5) The kit of claim 2 and further comprising one or more transmission line models ([0036];[0037]);
- (8) The topology of claim 6 comprising a definite current return path ([0005]-[0006]);
- (9), (38), (39) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters ([0032]-[0033]; [0037]);
- (11)-(14) The design topology wherein said topology comprises one or more signal wires and one or more shielding wires ([0008]; [0035]);
- (16), (18) The product further comprising instructions, cause said computer to create a design model of transmission lines ([0032]-[0033]; [0037]);
- (36), (41), (33) The method, wherein the step of designing comprises choosing from a set of predefined parameterized design topologies/cells ([0032]-[0033]; [0037]; [0041]-[0042]);
- (40) The method according to claim 32, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, timing requirements ([0041]-[0042]).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 2-7, 9 and 15-18 are rejected under 35 U.S.C. 102(b) as being unpatentable by Chao et al. (US Patent 5,031,111).

Chao discloses automated technique for the design of microwave and similar circuits using computer system including:

As to claims 2, 6, 15 and 17 Chao describes:

(2) An integrated circuit design kit/system comprising (col.4, ll.40-67; col.5, ll.1-10; col.9, ll.34-59):

means/tools for generating one or more circuit component topologies (col.1, ll.5-10; col.2, ll.24-54; col.4, ll.15-39); and

means/tools for designing one or more transmission line topologies, for analog and mixed signal (AMS) circuit (microwave and similar circuit) design (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(6) A design topology of AMS transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(15) A computer software product for designing an AMS integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said

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computer to create a design topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8);

(17) A computer software circuit design product for designing an AMS integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream) said circuit design product, said circuit design product comprising means for designing topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8 and ll.26-54);

As to claims 3-5, 7, 9, 16 and 18 Chao recites:

(3) The kit of claim 2 wherein said transmission line topologies are predefined (in a library) (col.5, ll.11-40);

(4) The kit of claim 2 further comprising one or more circuit component models (col.2, ll.37-67; col.3, ll.1-40);

(5) The kit of claim 2 and further comprising one or more transmission line models (col.2, ll.37-67; col.3, ll.1-40);

(7) The design topology of claim 6 wherein said topology is predefined (col.5, ll.11-40);

(9) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters (col.4, ll.15-39);

(16), (18) The product further comprising instructions, which when read by a computer, cause said computer to create a design model of transmission lines (col.2, ll.37-67; col.3, ll.1-40).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 6 is rejected under 35 U.S.C. 102(e) as being unpatentable by Pileggi et al. (US Patent 6,286,128).

As to claim 6 Pileggi discloses method for design optimization using logical and physical information including:

A design topology (net topology) of AMS transmission lines (mixed mode signals on RF transmission lines) (col.5, ll.62-67; col.6, ll.1-4; col.13, ll.46-58; col.14, ll.1-2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 6, 15 and 17 is rejected under 35 U.S.C. 102(e) as being unpatentable by Boyle et al. (US Patent 6,557,145).

As to claim 6 Boyle recites:

(6) A design topology (net topology) of AMS transmission lines (mixed mode signals on RF transmission lines) (col.11, ll.53-58; col.19, ll.36-50);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of transmission lines (col.3, ll.51-67; col.4, ll.1-4; col.11, ll.53-58; col.19, ll.36-50);

(17) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a design kit comprising a topology of critical interconnect lines (col.3, ll.51-67; col.4, ll.1-4; col.11, ll.53-58; col.19, ll.36-50).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 2-13, 15-18, 36-37, 38-40 and 30 are rejected under 35

U.S.C. 102(e) as being anticipated by Dansky et al. (US Patent 6,342,823).

Dansky discloses system and method for reducing calculation complexity of lossy, frequency-dependent transmission-line computation including:

As to claims 2, 6, 15, 17, 30 and 32 Dansky recites:

(2) An integrated circuit design kit comprising:

means for generating or more circuit components topologies (col.5, ll.19-24); and

means for designing one or more transmission lines topologies for analog and mixed signal (AMS) circuit design(Abstract; col.5, ll.19-24);

(6) A design topology of AMS transmission lines (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of transmission lines (Abstract; col.2, ll.36-49; col.3, ll.26-48; col.5, ll.22-24; col.6, ll.64-67 and col.8, ll.1-5);

(17) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a

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design kit comprising a topology of critical interconnect lines (Abstract; col.2, ll.36-49; col.3, ll.26-48; col.5, ll.19-24; col.6, ll.64-67 and col.8, ll.1-5);

(30) A method for designing integrated circuits wherein defining said chip architecture and a floor plan comprises defining critical interconnect wires (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67).

(32) A method for designing integrated circuit comprising:

(a) defining a chip architecture and a floor plan; (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(b) identifying one or more critical interconnect lines, and defining one or more transmission line topologies for said critical interconnect lines (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(c) determining a schematic design of said IC from said chip architecture floor plan and said transmission line topologies (col.5, ll.22-24 and ll.34-35);

(d) defining a physical layout of said IC at least from said chip architecture floor plan and said transmission line topologies (col.5, ll.19-24).

As to claims 3-5, 7-9, 11-13, 36, and 39-40 Dansky discloses:

(3), (7), (36) The kit of, wherein said interconnect line topologies are predefined (col.5, ll.21-31);

(4) The kit of claim 2 and further comprising one or more circuit components models (col.5, ll.22-24 and ll.34-35);

(5) The kit of claim 2 and further comprising one or more critical interconnect lines models (col.5, ll.22-24 and ll.34-35);

(8) The topology of claim 6 comprising a definite current return path (col.3, ll.34-37 and col.4, ll.31-36);

(9), (39) The topology of claim 6 wherein said topology is supplemented by a model comprising one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (col.2, ll.26-34 and col.3, ll.54-60);

(11) The topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires (col.2, ll.56-63);

(12) The topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires (col.3, ll.26-47);

(13) The topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire (col.3, ll.26-47);

(40) The method according to claim 19, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment and manual user selection (col.1, ll.17-19 and col.5, ll.21-31).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 2-9, 11-18, 30-35 and 36-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Voldman (US Patent 6,704,179).

As to claims 2, 6, 15, 17, 30-32, and 34-35 Voldman discloses:

(2) An integrated circuit design kit/system comprising:

means/tools for generating one or more circuit component topologies (col.2, ll.40-51); and

means/tools for designing one or more transmission line topologies (parameterized interconnections), for analog and mixed signal circuit (microwave and similar circuit) design (col.3, ll.42-67; col.4, ll.1-21);

(6) A design topology of analog and mixed signal transmission lines (col.3, ll.42-67; col.4, ll.1-21);

(15) A computer software product for designing an analog and mixed signal integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines (col.2, ll.25-51; col.3, ll.42-67; col.4, ll.1-21);

(17) A computer software circuit design product for designing an analog and mixed signal integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream)

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said circuit design product, said circuit design product comprising means for designing topology of transmission lines (col.2, ll.25-51; col.3, ll.42-67; col.4, ll.1-21);

(30) A method for designing analog and mixed signal integrated circuits wherein defining said chip architecture and a floor plan (physical design) comprises defining critical interconnect wires (design classes) (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(31) a system for integrated circuit design comprising:

means (tools/simulators/synthesizers) for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks (macros) and their locations are defined, and further including one or more analog and mixed signal transmission line (parameterized interconnects) topologies (col.6, ll.17-44; col.6, ll.55-67);

means (tools/simulators/synthesizers) for designing a schematic design at least including one or more circuit components and one or more transmission lines models (col.2, ll.25-51; col.6, ll.17-44); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more transmission line topologies (col.3, ll.41-67; col.4, ll.1-21; col.6, ll.17-44; col.6, ll.55-67);

(32) A method for designing integrated circuit comprising:

(a) defining a chip architecture and a floor plan (col.6, ll.17-44; col.6, ll.55-67);

(b) identifying one or more critical interconnect lines, and defining one or more analog and mixed signal transmission line topologies for said critical interconnect lines (col.3, ll.26-67; col.4, ll.1-21; col.5, ll.22-24 and col.6, ll.64-67);

(c) determining a schematic design of said IC from said chip architecture floor plan and said transmission line topologies (col.3, ll.26-67; col.4, ll.1-21; col.6, ll.17-44; col.6, ll.55-67);

(d) defining a physical layout of said IC at least from said chip architecture floor plan and said transmission line topologies (col.3, ll.41-67; col.4, ll.1-21; col.6, ll.17-44; col.6, ll.55-67);

(34) A system for integrated circuit design comprising:
means/tools for designing a schematic design at least including one or more circuit components and one or more analog and mixed signal transmission lines models, wherein said one or more transmission lines are models parameterized cells of one or more transmission lines topologies (col.2, ll.25-51; col.3, ll.42-67; col.4, ll.1-21);

(35) A method for designing integrated circuits (IC), said method comprising:
means (tools/simulators/synthesizers) for designing a schematic design (col.2, ll.25-51; col.6, ll.17-44); and

means (tools/simulators) for designing a physical layout including at least one or more circuit components and one or more analog and mixed signal transmission line topologies, wherein said one or more transmission line topologies are parameterized cells of transmission lines (col.3, ll.41-67; col.4, ll.1-21; col.6, ll.17-44; col.6, ll.55-67).

As to claims 3-5, 7-14, 16, 18, 33 and 36-41 Voldman recites:

(3), (7) The kit of, wherein said interconnect line topologies are predefined (col.3, ll.41-67; col.4, ll.1-21);

(4), (5), (6), (16), (18) The kit further comprising one or more circuit components models, critical interconnect lines models, transmission line topologies (col.3, ll.42-67; col.4, ll.1-21);

(8) The topology of claim 6 comprising a definite current return path (col.4, ll.38-61);

(9), (38), (39) The topology, wherein said topology is supplemented by a model comprising one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (col.2, ll.15-24);

(11)-(14) The topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires (col.6, ll.5-16);

(33), (36), (41) The method according, wherein said physical design comprises parameterized cells of said one or more transmission line topologies (col.3, ll.42-67; col.4, ll.1-21);

(37) The method of claim 32, wherein step b) comprises defining a set of design topologies (col.2, ll.40-51; col.3, ll.42-67; col.4, ll.1-21);

(40) The method according to claim 19, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment and manual user selection (col.4, ll.62-67; col.5, ll.1-9).

REMARKS

12. Examiner appreciates the detailed remarks offered by Applicants, however, he does not find them persuasive, because claims not recite these specific particular limitations. Applicants simply indicate and does not really provide support for his/her positions. The references cited each detail analog + mixed (analog and digital) signal usage. Further as indicated the references do read upon the claim language. For these reasons the prior rejections are maintained. However, Applicants' arguments are to look are well taken.

Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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